REMARKS

The following remarks are responsive to the June 24, 2005 Final Office Action. Claims 1, 6-8, and 10-19 remain as previously presented and Claims 2-5 and 9 remain as originally filed. Thus, Claims 1-19 are presented for further consideration.

Response to Rejection of Claims 1, 12, and 19 Under 35 U.S.C. § 102(b)

In the June 24, 2005 Final Office Action, the Examiner rejects Claims 1, 12, and 19 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,049,476 issued to Laudon et al. ("Laudon"). In particular, the Examiner cites Figure 4 of Laudon as disclosing each of the limitations of these claims.

Claim 1

Claim 1 recites (emphasis added):

> 1. A memory module comprising:
> a printed circuit board having a first lateral portion and a second lateral portion;
> a plurality of identical integrated circuits mounted in at least two rows onto at least one surface of the printed circuit board;
> a control logic bus connected to the plurality of identical integrated circuits; and
> a first register and a second register connected to the control logic bus, the first register addressing the identical integrated circuits located on the first lateral portion and **not addressing** the identical integrated circuits located on the second lateral portion, and the second register addressing the identical integrated circuits located on the second lateral portion and **not addressing** the identical integrated circuits located on the first lateral portion.

Applicants submit that Laudon does not disclose a "first register addressing the identical integrated circuits located on the first lateral portion and not addressing the identical integrated circuits located on the second lateral portion" or a "second register addressing the identical integrated circuits located on the second lateral portion and not addressing the identical integrated circuits located on the first lateral portion," as recited by Claim 1.

Referring to Figure 4, at col. 9, lines 30-51, Laudon discloses that (emphasis added):

> Address and control buffers 214, 216 receive 20-bits of address and control signals, labeled A[19:0], buffers the address and control signals, and provides the address and control signals to SDRAMs D0-D17 as follows. Address and control buffer 214 provides address and control signals (i.e., row address strobe, column address strobe, write enable and data mask) to left sides of bank portions 210, 212 (i.e., SDRAMs D0-D3 and D9-D12) via bus 113. In addition, **address and control buffer 214 provides a bank select signal (CS0_) and a clock enable signal (CKE0) to both the left and right sides of first bank portion 210** (i.e., SDRAMs D0-D8) via lines 117.

> Address and control buffer 216 provides address and control signals (i.e., row address strobe, column address strobe, write enable and data mask) to right sides of bank portion 210, 212 (i.e., SDRAMs D4-D8 and D12-D17) via bus 115. In addition, **address and control buffer 216 provides a bank select signal (CS1_) and a clock enable signal (CKE1) to both the left and right sides of second bank portion 212** (i.e., SDRAMs D9-D17) via lines 119. Address and control signals A[19:0] are described further below in Table 1.

As described by Table 1 of Laudon, these bank select signals and clock enable signals are included in the address and control signals labeled A[19:0], with the bank select signals being part of the data memory address. The above-quoted passage of Laudon teaches that each of the address and control buffers 214, 216 addresses **both** the left and right sides of the DIMM. Therefore, Applicants submit that Laudon does not teach a memory module having a "first register addressing the identical integrated circuits located on the first lateral portion and not addressing the identical integrated circuits located on the second lateral portion" or a "second register addressing the identical integrated circuits located on the second lateral portion and not addressing the identical integrated circuits located on the first lateral portion," as recited by Claim 1.

For the above-stated reasons, Applicants submit that Claim 1 is not anticipated by the teachings of Laudon. Applicants respectfully request that the Examiner withdraw the rejection of Claim 1 and pass Claim 1 to allowance.

Claim 12

Claim 12 recites (emphasis added):

> 12. A memory module comprising:
> a printed circuit board;
> a plurality of identical integrated circuits mounted in a first row and a second row onto at least one surface of the printed circuit board;
> a control logic bus connected to the plurality of identical integrated circuits; and
> a first register and a second register connected to the control logic bus, the first register addressing **only** the identical integrated circuits located in the first row and the second row of identical integrated circuits on a first lateral portion of the at least one surface of the printed circuit board, and the second register addressing **only** the identical integrated circuits located in the first row and the second row of identical integrated circuits on a second lateral portion of the at least one surface of the printed circuit board.

For reasons similar to those discussed above in relation to Claim 1, Applicants submit that Claim 12 includes limitations not taught by Laudon, so Claim 12 is not anticipated by Laudon. Applicants respectfully request that the Examiner withdraw the rejection of Claim 12 and pass Claim 12 to allowance.

Claim 19

Claim 19 recites (emphasis added):

> 19. A memory module comprising:
> a printed circuit board having a first lateral portion and a second lateral portion;
> a plurality of identical integrated circuits mounted on the printed circuit board in a first row and a second row;
> a control logic bus connected to the plurality of identical integrated circuits;
> a first register connected to the control logic bus, the first register addressing the identical integrated circuits located in the first row and the second row on the first lateral portion and **not addressing** the identical integrated circuits located in the first row and the second row on the second lateral portion; and
> a second register connected to the control logic bus, the second register addressing the identical integrated circuits located in the first row and the second row on the second lateral portion and **not addressing** the identical integrated circuits located in the first row and the second row on the first lateral portion.

For reasons similar to those discussed above in relation to Claim 1, Applicants submit that Claim 19 includes limitations not taught by Laudon so Claim 19 is not anticipated by Laudon. Applicants respectfully request that the Examiner withdraw the rejection of Claim 19 and pass Claim 19 to allowance.

Response to Rejection of Claims 10, 11, 13, and 14 Under 35 U.S.C. § 103(a)

In the June 24, 2005 Final Office Action, the Examiner rejects Claims 10, 11, 13, and 14 under 35 U.S.C. § 103(a) as being unpatentable over Laudon. The Examiner states that Laudon teaches all the limitations of these claims, except for the first lateral portion comprising a first lateral half of the printed circuit board or the second lateral portion comprising a second lateral half of the printed circuit board. However, the Examiner states that it would have been obvious to persons skilled in the art at the time the invention was made to arrive at these specific features, since it has been held that rearranging parts of an invention involves only routine skill in the art.

Each of Claims 10 and 11 depends from Claim 1, so each of Claims 10 and 11 includes all the limitations of Claim 1, as well as other limitations of particular utility. As discussed above, Laudon does not teach all the limitations of Claim 1, and Applicants submit that these limitations are not obvious in view of Laudon. Therefore, Applicants submit that Claims 10 and 11 are patentably distinguished from Laudon. Applicants respectfully request that the Examiner withdraw the rejection of Claims 10 and 11 and pass these claims to allowance.

Each of Claims 13 and 14 depends from Claim 12, so each of Claims 13 and 14 includes all the limitations of Claim 12, as well as other limitations of particular utility. As discussed above, Laudon does not teach all the limitations of Claim 12, and Applicants submit that these limitations are not obvious in view of Laudon. Therefore, Applicants submit that Claims 13 and 14 are patentably distinguished from Laudon. Applicants respectfully request that the Examiner withdraw the rejection of Claims 13 and 14 and pass these claims to allowance.

Response to Rejection of Claims 2-5 Under 35 U.S.C. § 103(a)

In the June 24, 2005 Final Office Action, the Examiner rejects Claims 2-5 under 35 U.S.C. § 103(a) as being unpatentable over Laudon in view of U.S. Patent No. 6,502,161 issued to Perego et al. ("Perego"). With regard to Claims 2, 4, and 5, the Examiner states that Laudon teaches all the limitations of these claims, except for the use of double data rate SDRAM and the use of 256-Megabit or 512-Megabit SDRAM, but that these limitations are taught by Perego and that it would be obvious to combine the features of Laudon and Perego. With regard to Claim 3, the Examiner also states that while neither Laudon nor Perego teaches the dimensions of the printed circuit board, changing the size of the printed circuit board is within the level of ordinary skill in the art.

As described above, Laudon does not teach all the limitations of Claim 1. Applicants submit that Perego does not teach or suggest all the limitations of Claim 1 which are missing from Laudon. Therefore, Claim 1 is patentably distinguished over Laudon in view of Perego.

Each of Claims 2-5 depends from Claim 1, so each of Claims 2-5 includes all the limitations of Claim 1, as well as other limitations of particular utility. Therefore, Applicants submit that Claims 2-5 are patentably distinguished from Laudon in view of Perego. Applicants respectfully request that the Examiner withdraw the rejection of Claims 2-5 and pass these claims to allowance.

Response to Rejection of Claims 6-9 and 15-18 Under 35 U.S.C. § 103(a)

In the June 24, 2005 Final Office Action, the Examiner rejects Claims 6-9 and 15-18 under 35 U.S.C. § 103(a) as being unpatentable over Laudon in view of U.S. Patent No. 6,594,167 issued to Yamasaki et al. ("Yamasaki"). The Examiner states that Laudon teaches all the limitations of these claims, except for the two rows having different orientation directions, but that these limitations are taught by Yamasaki and that it would be obvious to combine the features of Laudon and Yamasaki.

As described above, Laudon does not teach all the limitations of Claim 1 or of Claim 12. Applicants submit that Yamasaki does not teach or suggest all the limitations of Claim 1 or Claim 12 which are missing from Laudon. Therefore, Claim 1 and Claim 12 are patentably distinguished over Laudon in view of Yamasaki.

Each of Claims 6 and 8 depends from Claim 1, Claim 7 depends from Claim 6, and Claim 9 depends from Claim 8, so each of Claims 6-9 includes all the limitations of Claim 1, as well as other limitations of particular utility. Each of Claims 15 and 17 depends from Claim 12, Claim 16 depends from Claim 15, and Claim 18 depends from Claim 17, so each of Claims 15-19 includes all the limitations of Claim 12, as well as other limitations of particular utility. Therefore, Applicants submit that Claims 6-9 and 15-19 are patentably distinguished from Laudon in view of Yamasaki. Applicants respectfully request that the Examiner withdraw the rejection of Claims 6-9 and 15-19 and pass these claims to allowance.

Summary

For the foregoing reasons, Applicants submit that Claims 1-19 are in condition for allowance, and Applicants respectfully request such action.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: 8/25/05 By: _____

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